CLAIMS

What is claimed is:

1. A method of determining the source of a processor reset in a system having a processor and a plurality of processor reset sources, comprising the steps of:

coupling the plurality of processor reset sources to a corresponding plurality of latches;

setting one of the latches in response to a processor reset generated by a corresponding one of the processor resets;

writing logic high to a first register bit of a read register and designated by the one latch;

rebooting the processor; and

reading the first register bit from the read register to determine which of the reset sources generated the processor reset.

2. A method of claim 1, further comprising the step of resetting the read register to determine a subsequent processor reset source.

3. A method of claim 2, wherein the step of resetting the read register comprises resetting the first register bit.

4. A method of claim 2, wherein the step of resetting the read register comprises the step of writing logic high to a second register bit of a write register and corresponding to the first register bit.

5. A method of claim 4, wherein the step of resetting the read register comprises the step of resetting the one latch through the logic high register bit of the write register.

6. A method of claim 5, further comprising the step of writing logic low to the first register bit and through the one latch.

7. A method of claim 6, further comprising the step of clear enabling the latches.

8. A method of claim 7, wherein the step of clear enabling the latches comprises the step of writing logic low to register bits of the write register.

9. A method of claim 1, wherein the step of coupling the plurality of processor reset sources to a corresponding plurality of latches comprises coupling the plurality of processor reset sources to a corresponding plurality of RS latches.

10. Logic apparatus for coupling with a processor and a plurality of processor reset sources to determine which of the sources generated a processor reset, comprising:

a plurality of latches, each of the latches being uniquely coupled to one of the reset sources, each of the reset sources setting a corresponding latch when generating a processor reset; and

a read register coupled to the latches, each of the latches setting logic high in a corresponding read register bit of the read register in response being set by a processor reset, the processor reading the register bit after rebooting to determine which of the sources generated the reset.

11. Apparatus of claim 10, further comprising a write register, the read register and processor cooperating to set logic high in a write register bit of the write register that corresponds to the read register bit, the write register being coupled with the latches to reset one of the latches set by the processor reset.

12. Apparatus of claim 11, the one latch resetting logic low to the read register bit in response to being reset by the write register.

13. Apparatus of claim 11, the processor writing logic low to each write register bit of the write register to clear enable the latches.

14. Apparatus of claim 11, wherein at least one of the write and read registers comprises an 8-bit register.

15. Apparatus of claim 10, wherein at least one of the latches comprises a RS latch.

16. In a processor providing functions to a system having a plurality of processor reset sources, the improvement comprising a read register, coupled to the reset sources, for setting one of its read register bits in response to a processor reset by one of the reset sources, the processor reading the one read register bit upon rebooting to determine which of the sources generated the processor reset.

17. In a processor of claim 16, the further improvement comprising a first logic section having a plurality of latches, each of the latches being uniquely coupled to one of the reset sources, each of the reset sources setting a corresponding latch when generating a processor reset, the corresponding latch setting the one read register bit to logic high.

18. In a processor of claim 17, the further improvement comprising a second logic section having a write register for resetting one of the latches set by the processor reset.

19. In a processor of claim 18, the further improvement comprising a third logic section for writing logic low to register bits of the write register to clear enable the latches.

20. In a processor of claim 18, the further improvement wherein the one latch clears the one read register bit in response to being reset by the write register.